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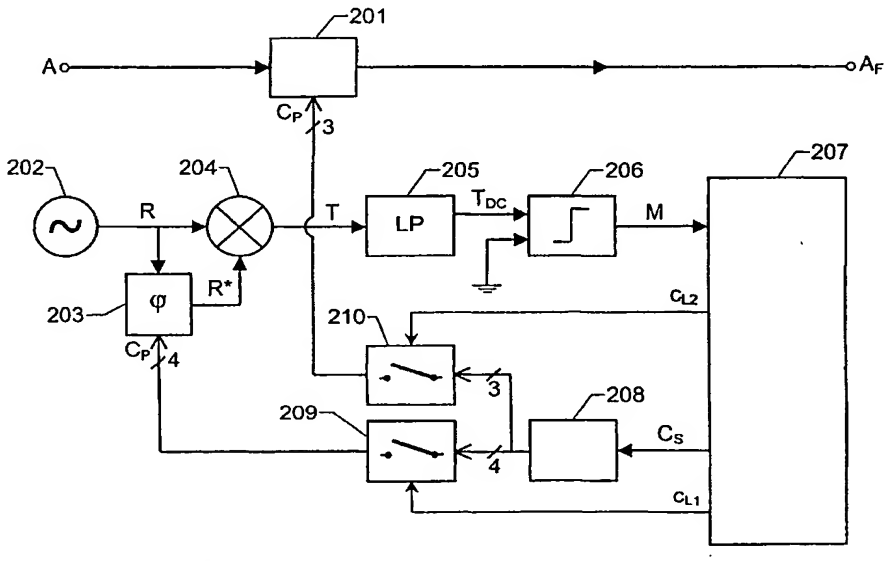
(54) Title: FILTER TRIMMING



(57) Abstract: The invention relates to a trimming of analogue filters (201) in integrated circuits by means of an automatic adjusting circuit. A local osciallator (202) in the automatic adjusting circuit provides a periodic reference signal (R) to an adjustable phase shifter (203), which on basis thereof, produces a periodic phase shifted signal (R*). A phase detector (204) receives both the periodic reference signal (R) and the phase shifted periodic signal (R*) and produces a test signal (T) in response to a phase difference between the periodic reference signal (R) and the periodic phase shifted signal (R*). A lowpass filter (205) receives the test signal (T) and generates a level signal (T_{DC}) representing a DC component of the test signal (T). A comparator (206) receives the test signal (T_{DC}) and produces an observation signal (M) on basis of the level signal (T_{DC}) relative a reference level, e.g. representing a zero voltage. A digital signal processor (207) produces a primary control signal (C_S), having a serial format , on basis of the observation signal (M). A serial-to-parallel converter (208) converts the primary control signal (C_S) into a control signal (C_P) having a parallel signal format.The control signal (C_P) influences a magnitude of at least one component value in the adjustable phase shifter (203) and is allocated such value that the phase shift between the periodic reference signal (R) and the periodic phase shifted signal (R*) attains a calibrated value being as close as possible to a desired value. A latch (210) forwards at least one signal element of the control signal (C_P) for setting of at least one component value in the analogue filter (201) in accordance with a setting of the at least one component value in the adjustable phase shifter (203) which produces the calibrated value.

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Filter Trimming

THE BACKGROUND OF THE INVENTION AND PRIOR ART

The present invention relates generally to trimming of analogue filters in integrated circuits. More particularly the invention relates to a method for automatically altering a magnitude of at least one component value in an analogue filter according to the preamble of claim 1 and an automatic adjusting circuit for calibrating an analogue filter in an integrated circuit according to claim 15. The invention also relates to a computer program according to claim 13 and a computer readable medium according to claim 14.

The manufacturing process for integrated circuits generally causes a degree of uncertainty with respect to the component values of specific component types. Integrated passive components, such as capacitors and resistors demonstrate undesirable variations in component values, so-called process variations. The value of an actual RC-product in a filter may deviate as much as 30 – 40% from a nominal value as a consequence of the process variations. Various attempts have already been made to compensate for these detrimental effects.

For instance, the patent document JP, 11274895 discloses a signal processing circuit that is capable of making up for variations of integrated resistors and capacitors by means of adjustable digital filters. A filter coefficient switching means sets the filter coefficient values in a set of digital filters from a pre-defined coefficient table. The filter coefficient switching means

chooses such coefficient values that any variation in a signal processing circuit being due to the variation of a semiconductor manufacturing process is compensated for.

The U.S. patent No. 5,179,727 describes an automatic adjusting circuit for an analogue filter on a semiconductor chip. The adjusting circuit controls the filter's parameters such that its centre frequency becomes equal to a reference frequency. The automatic adjusting circuit includes a first phase detector and calibrating filter for coarse frequency tuning and a second phase detector and calibrating filter for fine frequency tuning. The first phase detector produces a signal based on a phase difference between the reference signal and the reference signal filtered through the first calibrating filter, having a low selectivity, and the second phase detector produces a signal based on a phase difference between the reference signal and the reference signal filtered through the second calibrating filter, having a high selectivity. A composite signal is then formed by combining the output signals from both the phase detectors. A DC component of the composite signal is, on one hand, fed back as a control signal to the calibrating filters. On the other hand, the DC component controls the centre frequency of the analogue filter to be controlled to a predetermined ratio with respect to the reference frequency signal by automatically adjusting the centre frequency of the calibrating filters to be equal to the reference frequency signal.

The solution according to the former reference involves digital filtering in series with the analogue filter. Digital filters, however, always cause power losses and introduce a degree of distortion into the signal path. Digital filters are therefore undesired if they can be avoided.

The latter reference, conversely, tunes itself by an analogue manner to a desired centre frequency. This is, of course, a flexible solution that allows a designer to utilise one and the same filter for a multitude of applications in which different

filtering characteristics may be demanded. However, the solution involves active filters that per se are relatively noisy and non-linear. This in turn causes distortion and deteriorates the filter performance, which of course, is adverse.

Consequently, the prior art presents various means to either directly compensate for process variations of integrated component values or to alter an analogue filter's filtering characteristics and thus indirectly compensate for any process variations. However, the proposed solutions are associated with various unwanted side effects, such as power loss, distortion, noise or combinations thereof.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to alleviate the problems above and thus provide an improved solution for handling process variations of integrated component values.

According to one aspect of the invention the object is achieved by a method for automatically altering a magnitude of at least one component value in an analogue filter as initially described, which is characterised by the integrated circuit comprising an adjustable phase shifter for receiving a periodic reference signal. Based on this reference signal the adjustable phase shifter produces a periodic phase shifted signal. The method involves adjusting a magnitude of at least one component value in the adjustable phase shifter in response to a control signal, such that the phase shift between the periodic reference signal and the periodic phase shifted signal attains a calibrated value, which is as close as possible to a desired value, for instance 90°. The control signal is in turn generated on basis of a test signal that is produced by a phase detector, which receives the periodic reference signal and the phase shifted periodic reference signal. The method finally involves setting at least one component value in the analogue filter in accordance with a

setting of the at least one component value in the adjustable phase shifter, which produces the calibrated value.

According to another aspect of the invention these objects are achieved by a computer program directly loadable into the internal memory of a digital computer, comprising software for controlling the method described in the above paragraph when said program is run on a computer, for instance, a digital signal processor (DSP).

According to yet another aspect of the invention these objects are achieved by a computer readable medium, having a program recorded thereon, where the program is to make a computer, such as a DSP, perform the method described in the penultimate paragraph above.

According to an additional aspect of the invention the object is achieved by an automatic adjusting circuit for calibrating an analogue filter in an integrated circuit. The automatic adjusting circuit includes an adjustable phase shifter that receives a periodic reference signal, and on basis thereof, produces a periodic phase shifted signal. The automatic adjusting circuit also includes a phase detector for receiving the periodic reference signal and the phase shifted periodic signal, and producing a test signal in response to a phase difference between the periodic reference signal and the periodic phase shifted signal. Moreover, the automatic adjusting circuit includes means for producing a control signal on basis of the test signal. The control signal influences a magnitude of at least one component value in the adjustable phase shifter and it is allocated such value that the phase shift between the periodic reference signal and the periodic phase shifted signal attains a calibrated value being as close as possible to a desired value. Finally, the automatic adjusting circuit comprises means for setting the at least one component value in the adjustable filter in accordance with a setting of the at least one component value

in the adjustable phase shifter, which produces the calibrated value.

The invention thereby provides an efficient solution, which makes it possible to handle unavoidable process variations of integrated component values.

The invention also offers a competent possibility for continuous compensation for any variations in component values due to temperature variations.

Moreover, the proposed solution includes standardised and relatively uncomplicated building blocks. The invention therefore constitutes an attractive alternative also from a cost and a robustness point-of-view.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is now to be explained more closely by means of preferred embodiments, which are disclosed as examples, and with reference to the attached drawings.

Figure 1 shows a circuit diagram over an analogue filter according to a first embodiment of the invention,

Figure 2 shows a block diagram over an automatic adjusting circuit for calibrating an analogue filter according to a first embodiment of the invention,

Figure 3 shows a circuit diagram over an adjustable phase shifter according to the first embodiment of the invention, and

Figure 4 shows a circuit diagram over analogue filter according to a second embodiment of the invention, and

Figure 5 illustrates, by means of a flow diagram, an embodiment of the method according to the invention.

DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

As mentioned initially, the value of an actual RC-product in an integrated filter may deviate up to ±40% from a corresponding nominal value due to variations in the semiconductor manufacturing process. Obviously, deviations of such magnitude cannot be tolerated, since they result in very unpredictable filter characteristics. Furthermore, the value of the RC-product may deviate over time in consequence of temperature variations and thus require a continuous or repeated compensation.

Figure 1 shows a circuit diagram over an analogue lowpass filter 201, according to an embodiment of the invention. Having the process variations in mind, the filter 201 is prepared in advance with a set of controllable switches s_{11}, s_{12} and s_{13}, which each controls a particular capacitor C_{11}, C_{12} and C_{13} respectively, such that any combination of individual capacitors C_{11} - C_{13} may be included electrically in the filter circuit in addition to a minimum capacitance C_{min}. According to a preferred embodiment of the invention, each of the switchable capacitors has a different component value, for instance, C_{11} = 1,0C, C_{12} = 2,0C and C_{13} = 4,0C. Depending on how the controllable switches s_{11}, s_{12} and s_{13} are set, the total nominal capacitance value can thus be varied from C_{min} to C_{min}+7,0C. The actual capacitance value may, of course, deviate from the nominal capacitance value due to the process variations. However, the controllable switches s_{11} - s_{13} provide a considerable degree of freedom to vary also the actual capacitance value. Especially, the actual capacitance value is expected to be adjustable to a value that is sufficiently close to the nominal capacitance value. Even if also the component of one or more resistors R_1 included in the filter 201

deviate from corresponding nominal values, the controllable switches s_{11} - s_{13} make it possible to adjust the RC product to an acceptable value.

By assigning an adequate set of signal elements c_{P11} – c_{P13} in a control signal C_P, the controllable switches s_{11} - s_{13} can allocate a value to the RC product $(R_1 \times (s_{11}C_{11}+s_{12}C_{12}+s_{13}C_{13}+C_{min})$, where $s_i=1 \leftrightarrow$ closed switch and $s_i=0 \leftrightarrow$ open switch) which is sufficiently close to a desired nominal value. Consequently, an analogue input signal A fed through the lowpass filter 201 will produce an analogue output signal A_F in accordance with the filter design.

Nevertheless, it is not trivial to find the set of signal elements c_{P11} – c_{P13} in the control signal C_P that generates the desired RC product value. Therefore, an automatic adjusting circuit is attached to the analogue filter 201. According to a preferred embodiment of the invention, the automatic adjusting circuit and the analogue filter 201 are integrated onto one and the same circuit chip, such that they are both exposed to the same process variation. However, any other circuits, units or components involved may be located either on the same or on a different circuit chip.

Figure 2 shows a block diagram over an automatic adjusting circuit for calibrating the analogue filter 201 by means of the control signal C_P according to an embodiment of the invention. A local oscillator 202 produces a periodic reference signal R of a particular frequency. The periodic reference signal R is fed both to a phase detector 204 and to an adjustable phase shifter 203, whose phase shift with respect to the input signal depends on the value of the control signal C_P. The adjustable phase shifter 203 produces a periodic phase shifted signal R* based on the periodic reference signal R. The phase detector 204 receives both the periodic reference signal R and the phase shifted periodic signal R*. The phase detector 204 generates a test

signal T in response to a phase difference between the periodic reference signal R and the periodic phase shifted signal R*.

Provided that an optimal (or desired) setting of the adjustable phase shifter 203 corresponds to a phase shift between the periodic reference signal R and the phase shifted periodic signal R* equal to one quarter of a full period of the periodic reference signal R (i.e. 90° or $\pi/2$ radians), the phase detector 204 can be made of a multiplier. A zero valued test signal T thus indicates an ideal setting of the adjustable phase shifter 203 and consequently also an optimal control signal C_P. In principal, any phase shift between the periodic reference signal R and the phase shifted periodic signal R* can be regarded as an ideal value. However, it is preferable to choose a local oscillator 202 that produces a periodic reference signal R of such frequency relative the nominal component values, that an ideal setting of the adjustable phase shifter 203 implies a 90° phase difference between the periodic reference signal R and the phase shifted periodic signal R*. The phase detector 204 may then namely be a comparatively simple element, such as a multiplier.

A lowpass filter 205 receives the test signal T and produces in response thereto a level signal T_{DC}, which represents a direct voltage component of the test signal T. Minor deviations from an otherwise stable value (which ideally is zero) of the test signal T are thereby eliminated. Any other integrating elements besides a lowpass filter may, of course, be utilised in alternative embodiments of the invention. For instance, a purely capacitive element of suitable magnitude may constitute the lowpass filter 205.

A comparator 206 receives the level signal T_{DC} and produces an observation signal M on basis of the level signal T_{DC} relative a reference level, which for instance represents a zero voltage. The observation signal M is fed to a digital signal processor 207 for evaluation. The reference level received by the comparator 206 is chosen relative the ideal setting of the adjustable phase

shifter 203 and the phase detector 204, such that the smaller the absolute value of the observation signal M the better the adjustable phase shifter setting (and thus also the control signal C_P value). The digital signal processor 207 registers and stores any incoming observation signal M in an internal buffer memory.

Figure 3 shows a circuit diagram over an adjustable phase shifter according to the first embodiment of the invention. As can be seen in the figure, the adjustable phase shifter 203, in similarity with the analogue lowpass filter 201, contains a set of controllable switches s_{20}, s_{21}, s_{22} and s_{23}, which each controls a particular capacitor C_{20}, C_{21}, C_{22} and C_{23} respectively, such that any combination of individual capacitors C_{20} – C_{23} may be included electrically in a filter circuit in addition to the minimum capacitance C_{min}. The state of each controllable switch s_{20} - s_{23} is in turn determined by the value of the signal elements c_{P10} – c_{P13} in the control signal C_P.

Depending on the number of controllable switches s_{20}, s_{21}, s_{22} and s_{23} in the adjustable phase shifter 203, the signal elements c_{P10} – c_{P13} may be arranged according to a particular number of different combinations. The control signal C_P may thus attain the same number of different values. For instance, four controllable switches s_{20} - s_{23} result in 2^4=16 different values 0000 – 1111 of the control signal C_P. Given the nominal relationship in capacitance values C_{20} = 0,5C, C_{21} = 1,0C, C_{22} = 2,0C, C_{23} = 4,0C, the control signal C_P determines the nominal RC-product value according to table 1 below.

C_P				**RC-product** ($R_2 \times C_{tot}$)
c_{P13}	c_{P12}	c_{P11}	c_{P10}	[ΩF]
0	0	0	0	R_2C_{min}
0	0	0	1	$R_2(C_{min}+0,5)$
0	0	1	0	$R_2(C_{min}+1,0)$
0	0	1	1	$R_2(C_{min}+1,5)$
0	1	0	0	$R_2(C_{min}+2,0)$
0	1	0	1	$R_2(C_{min}+2,5)$

0	1	1	0	$R_2(C_{min}+3,0)$
0	1	1	1	$R_2(C_{min}+3,5)$
1	0	0	0	$R_2(C_{min}+4,0)$
1	0	0	1	$R_2(C_{min}+4,5)$
1	0	1	0	$R_2(C_{min}+5,0)$
1	0	1	1	$R_2(C_{min}+5,5)$
1	1	0	0	$R_2(C_{min}+6,0)$
1	1	0	1	$R_2(C_{min}+6,5)$
1	1	1	0	$R_2(C_{min}+7,0)$
1	1	1	1	$R_2(C_{min}+7,5)$

Table 1

Either the digital signal processor 207 systematically steps through the 16 control signal values C_P from 0000 to 1111 and stores a corresponding observation signal value M, or the digital signal processor 207 allocates values to the control signal C_P according to an alternative sequence, via which an optimal control signal C_P can be determined without necessarily stepping through all the 16 steps.

A first latch 209, being controlled by means of a first command signal c_{L1} from the digital signal processor 207, is closed when a the control signal C_P value has been updated, such that the control signal C_P value can be fed to the adjustable phase shifter 203 and the digital signal processor 207 can register a new observation signal value M. The digital signal processor 207 delivers a primary control signal value C_S, on a serial format, corresponding to a control signal value C_P to a serial-to-parallel converter 208. The serial-to-parallel converter 208 then produces the control signal C_P, having a parallel signal format, based on the primary control signal C_S.

According to an alternative embodiment of the invention, the digital signal processor 207 delivers the control signal value C_P directly on a parallel format being adapted to the analogue filter 201 and the adjustable phase shifter 203.

According to other alternative embodiments of the invention, one or both of the units 206 and 208 are realised by functions within the digital signal processor 207. The digital signal processor 207 generates a control signal C_P, in response to the observation signal M based on the following conditions.

According to other alternative embodiments of the invention, the comparator 206 is replaced by an A/D-converter that, as an alternative to the observation signal M, delivers a digitised level signal T_{DC} to the digital signal processor 207 for evaluation.

The digital signal processor 207 thus derives an optimal control signal value C_P that results in the smallest absolute value of the observation signal M. The digital signal processor 207 feeds a primary control signal value C_S representing the optimal control signal value C_P to a serial-to-parallel converter 208. The serial-to-parallel converter 208 produces a corresponding control signal C_P on basis of the primary control signal C_S. A second latch 210 being controlled by means of a second command signal c_{L2} from the digital signal processor 207, is closed such that the control signal C_P is forwarded to the analogue filter 203 whose controllable switches $s_{11} - s_{13}$ are set in accordance with the optimal control signal value C_P.

Provided that the process variation of the components in the analogue lowpass filter 201 is substantially the same (with respect to component type and magnitude) as the process variation of the components in the adjustable phase shifter 203, the setting of the controllable switches $s_{11} - s_{13}$ that accords with the optimal control signal value C_P is expected to bring about a desired filtering of the analogue input signal A into the analogue output signal A_F, irrespective of any process variation when manufacturing the semiconductor chip onto which the circuitry is integrated.

According to a preferred embodiment of the invention, the adjustable phase shifter 203 includes a controllable switch s_{20}

respective capacitor C_{20}, in addition to the total number of controllable switches s_{11}, - s_{13} in the analogue filter 201. This improves the possibility to achieve an optimal control signal value C_P. The closing of a controllable switch s_{21} for a capacitor C_{21}, corresponding to a smallest capacitance value C_{11} = 1,0C in the analogue filter 201, may namely cause a somewhat too large phase shift while the opening of the same switch s_{21} may cause a somewhat too small phase shift. It is generally difficult for the digital signal processor 207 to determine whether a closed or opened switch s_{21} provides the best result. However, the extra controllable switch s_{20} and capacitor C_{20} (preferably having a nominal capacitance value C_{20} = 0,5C, i.e. half the magnitude of the smallest capacitance value C_{11} = 1,0C in the analogue filter 201) make it possible to resolve determining which position of the switch s_{21} that provides the best result.

Figure 4 shows a circuit diagram over an analogue filter according to a second embodiment of the invention, wherein both a resistance value and a capacitance value can be altered. In the illustrated example, the control signal C_P has six signal elements c_{P11} – c_{P16}, of which the first three c_{P11} – c_{P13} control a respective switch s_{11} – s_{13} for a particular resistor R_{11} – R_{13}. All the resistors R_{11} – R_{13} are coupled in parallel with a fix resistor R_{max}, such that the total resistance value can be varied from $(R_{max}^{-1}+R_{11}^{-1}+R_{12}^{-1}+R_{13}^{-1})^{-1}$ to R_{max}. Correspondingly, the last three signal elements c_{P14} – c_{P16} in the control signal C_P control a respective switch s_{14} – s_{16} for a particular capacitor C_{14} – C_{16}. being coupled in parallel with a fix capacitor C_{min}, such that the total capacitance value can be varied from C_{min} to $(C_{min}+C_{14}+C_{15}+C_{16})$. Consequently, depending on the individual states of the signal elements c_{P11} – c_{P16}, the filter's RC-product can thus be varied in 2^6=64 steps between $(R_{max}^{-1}+R_{11}^{-1}+R_{12}^{-1}+R_{12}^{-1})^{-1}C_{min}$ and $R_{max}(C_{min}+C_{14}+C_{15}+C_{16})$.

The analogue filter according to this second embodiment of the invention can also be calibrated by means of the automatic adjusting circuit shown in figure 2. However, it is preferable that

the adjustable phase shifter instead includes five resistors R_{20}, R_{21}, R_{22}, R_{23}, and R_{max} having nominal values $R_{20} = 0{,}5R_{11}$, $R_{21} = R_{11}$, $R_{22} = R_{12}$, $R_{23} = R_{13}$ and R_{max} respectively and five capacitors C_{24}, C_{25}, C_{26}, C_{27}, and C_{min} having nominal values $C_{24} = C_{14}$, $C_{25} = C_{15}$, $C_{26} = C_{16}$, $C_{27} = 0{,}5C_{14}$ and C_{min} respectively. Analogously, the control signal C_P should then preferably include eight signal elements $c_{P10} - c_{P17}$.

In order to sum up, an embodiment of the proposed method for automatically altering a magnitude of at least one component value in an integrated analogue filter will now be described with reference to a flow diagram in the figure 5.

A first step 501, generates a periodic reference signal R, which is received in a second step 502. This step produces a phase shifted periodic reference signal R* on basis of the periodic reference signal R. A subsequent step 503, generates a test signal T from a phase difference φ between the periodic reference signal R and the phase shifted periodic reference signal R*. A following step 504, delivers a control signal C_P on basis of the test signal T. The control signal value C_P depends on the test signal T according to what has been described above, and may e.g. be produced according to the procedure disclosed with reference to the figures 1 – 3.

A step 505 then adjusts the magnitude of at least one component value in the adjustable phase shifter, such that the phase difference φ attains a calibrated value as close as possible to a desired value, for instance 90°. The at least one component value is varied systematically by means of the control signal C_P. After having found a control signal value C_P that generates the calibrated value, a final step 506 sets at least one component value in an analogue filter in accordance with the associated control signal value C_P. This calibrates the analogue filter, such that its filtering characteristics becomes as close as possible to the designed parameters, irrespective of any variations due the manufacturing process.

It should be noted that the steps 501 – 503 are performed continuously or at least periodically, and without direct control or involvement of a command unit (such as a digital signal processor). However, the steps 504 – 506 are executed at discrete moments in time and under direct control of a command unit.

All of the process steps, as well as any sub-sequence of steps, described with reference to the figure 5 above may be controlled by means of a computer program, for instance, a digital signal processor algorithm, being directly loadable into the internal memory of a general computer, a digital signal processor, a baseband processor or an ASIC (Application Specific Integrated Circuit), which includes appropriate software for controlling the necessary steps when the program is run on a computer/digital signal processor. The computer program can likewise be recorded onto arbitrary kind of computer readable medium.

The term "comprises/comprising" when used in this specification is taken to specify the presence of stated features, integers, steps or components. However, the term does not preclude the presence or addition of one or more additional features, integers, steps or components or groups thereof.

The invention is not restricted to the described embodiments in the figures, but may be varied freely within the scope of the claims.

It should particularly be noted that the invention is not restricted to any specific relationships between the respective integrated component values. Thus, the invention is equally well applicable to any component value ratios different from those exemplified above.

Claims

1. A method for automatically altering a magnitude of at least one component value (C_{11} - C_{13}; R_{11} – R_{13}, C_{14} - C_{16}) in an analogue filter (201) in an integrated circuit, the integrated circuit comprising a phase detector (204) for determining a present characteristic of the analogue filter (201) relative a desired characteristic, the method involving:

receiving a periodic reference signal (R) and a phase shifted periodic signal (R*) in the phase detector (204) and producing a test signal (T) in response to a phase difference between the periodic reference signal (R) and the periodic phase shifted signal (R*), **characterised by**

the integrated circuit comprising an adjustable phase shifter (203) for receiving the periodic reference signal (R) and on basis thereof producing the periodic phase shifted signal (R*), the method further involving:

altering a magnitude of at least one component value (C_{20} - C_{23}) in the adjustable phase shifter (203) in response to a control signal (C_P), such that the phase shift between the periodic reference signal (R) and the periodic phase shifted signal (R*) attains a calibrated value which is as close as possible to a desired value, the control signal (C_P) being generated on basis of the test signal (T), and

setting the at least one component value (C_{11} - C_{13}; R_{11} – R_{13}, C_{14} - C_{16}) in the analogue filter (201) in accordance with a setting of the at least one component value (C_{20} - C_{23}) in the adjustable phase shifter (203) which produces the calibrated value.

2. A method according to claim 1, **characterised by** the desired value corresponding to a quarter of a full period of the periodic reference signal (R).

3. A method according to any one of the claims 1 or 2, **characterised by** generating a level signal (T_{DC}) representing a direct voltage component of the test signal (T).

4. A method according to claim 3, **characterised by** producing the level signal (T_{DC}) by lowpass filtering the test signal (T).

5. A method according to any one of the claims 3 or 4, **characterised by** producing an observation signal (M) on basis of the level signal (T_{DC}) by comparing the level signal (T_{DC}) with a reference level.

6. A method according to claim 5, **characterised by** the reference level representing a zero voltage.

7. A method according to any one of the claims 5 or 6, **characterised by** producing a primary control signal (C_S) on basis of the observation signal (M), the primary control signal (C_S) in turn forming a basis for the control signal (C_P).

8. A method according to claim 7, **characterised by** the producing of the primary control signal (C_S) involving digital processing.

9. A method according to any one of the claims 7 or 8, **characterised by** receiving the primary control signal (C_S) in a serial signal format and generating, on basis thereof, the control signal (C_P) having a parallel signal format.

10. A method according to any one of the claims 1 - 9, **characterised by** the control signal (C_P) designating a setting of at least one first switch (s_{20} - s_{23}) in the adjustable phase shifter (203), each first switch (s_{20} - s_{23}) controlling a particular component value (C_{20} - C_{23}).

11. A method according to any one of the claims 1 - 10, **characterised by** the control signal (C_P) designating a setting of at least one second switch (s_{11} – s_{13}; s_{11} – s_{16}) in the analogue filter (201), each second switch (s_{11} – s_{13}; s_{11} – s_{16}) controlling a particular component value (C_{11} - C_{13}; R_{11} – R_{13}, C_{14} - C_{16}).

12. A method according to claim 11, **characterised by** positioning at least one second switch (s_{11} – s_{13}) controlling a component of a particular nominal component value in accordance with a positioning of at least one of the at least one first switch (s_{20} - s_{23}) controlling a component of a nominal component value being equal to the particular nominal component value.

13. A computer program directly loadable into the internal memory of a digital computer, comprising software for controlling the steps of any of the claims 1 – 12 when said program is run on a computer.

14. A computer readable medium, having a program recorded thereon, where the program is to make a computer control the steps of any of the claims 1 – 12.

15. An automatic adjusting circuit for calibrating an analogue filter (201) in an integrated circuit, comprising

an adjustable phase shifter (203) for receiving a periodic reference signal (R) and on basis thereof producing a periodic phase shifted signal (R*),

a phase detector (204) for receiving the periodic reference signal (R) and the phase shifted periodic signal (R*) and producing a test signal (T) in response to a phase difference between the periodic reference signal (R) and the periodic phase shifted signal (R*),

means (205 - 208) for producing a control signal (C_P) on basis of the test signal (T), the control signal (C_P) influencing a magnitude of at least one component value (C_{20} - C_{23}) in the adjustable phase shifter (203) and being allocated such value that the phase shift between the periodic reference signal (R) and the periodic phase shifted signal (R*) attains a calibrated value being as close as possible to a desired value, and

means (208, 210) for setting the at least one component value (C_{11}, C_{12}; C_{13}) in the analogue filter (201) in accordance with a setting of the at least one component value (C_{20} - C_{23}) in the adjustable phase shifter (203) which produces the calibrated value.

16. An automatic adjusting circuit according to claim 15, **characterised in that** it comprises a lowpass filter (205) for generating a level signal (T_{DC}) representing a direct voltage component of the test signal (T).

17. An automatic adjusting circuit according to claim 16, **characterised in that** it comprises a comparator (206) for producing an observation signal (M) on basis of the level signal (T_{DC}) relative a reference level.

18. An automatic adjusting circuit according to claim 17, **characterised in that** the reference level represents a zero voltage.

19. An automatic adjusting circuit according to any one of the claims 17 or 18, **characterised in that** it comprises a digital signal processor (207) for producing a primary control signal (C_S) on basis of the observation signal (M), the primary control signal (C_S) in turn forming a basis for the control signal (C_P).

20. An automatic adjusting circuit according to claim 19, **characterised in that** it comprises a serial-to-parallel converter (208) for receiving the primary control signal (C_S) according to a serial signal format and producing the control signal (C_P) having a parallel signal format.

21. An automatic adjusting circuit according to any one of the claims 15 - 20, **characterised in that** the control signal (C_P) includes at least one signal element ($c_{P10} - c_{P13}$), which each is adapted for designating a setting of at least one first switch (s_{20} - s_{23}) in the adjustable phase shifter (203), each first switch (s_{20} - s_{23}) controlling a particular component value (C_{20} - C_{23}).

22. An automatic adjusting circuit according to any one of the claims 15 - 21, **characterised in that** the control signal (C_P) includes at least one signal element ($c_{P11} - c_{P13}$; $c_{P11} - c_{P16}$), which each is adapted for designating a setting of at least one second switch ($s_{11} - s_{13}$; $s_{11} - s_{16}$) in the analogue filter (201), each second switch ($s_{11} - s_{13}$; $s_{11} - s_{16}$) controlling a particular component value (C_{11} - C_{13}; $R_{11} - R_{13}$, C_{14} - C_{16}).

23. An automatic adjusting circuit according to claim 22, **characterised in that** the analogue filter (201) receives the control signal (C_P) such that the at least one signal element ($c_{P11} - c_{P13}$; $c_{P11} - c_{P16}$) influences the at least one second switch ($s_{11} - s_{13}$; $s_{11} - s_{16}$) controlling a component of a particular nominal component value to be positioned in

accordance with a positioning of at least one of the at least one first switch (s_{20} - s_{23}) controlling a component of a nominal component value being equal to the particular nominal component value.

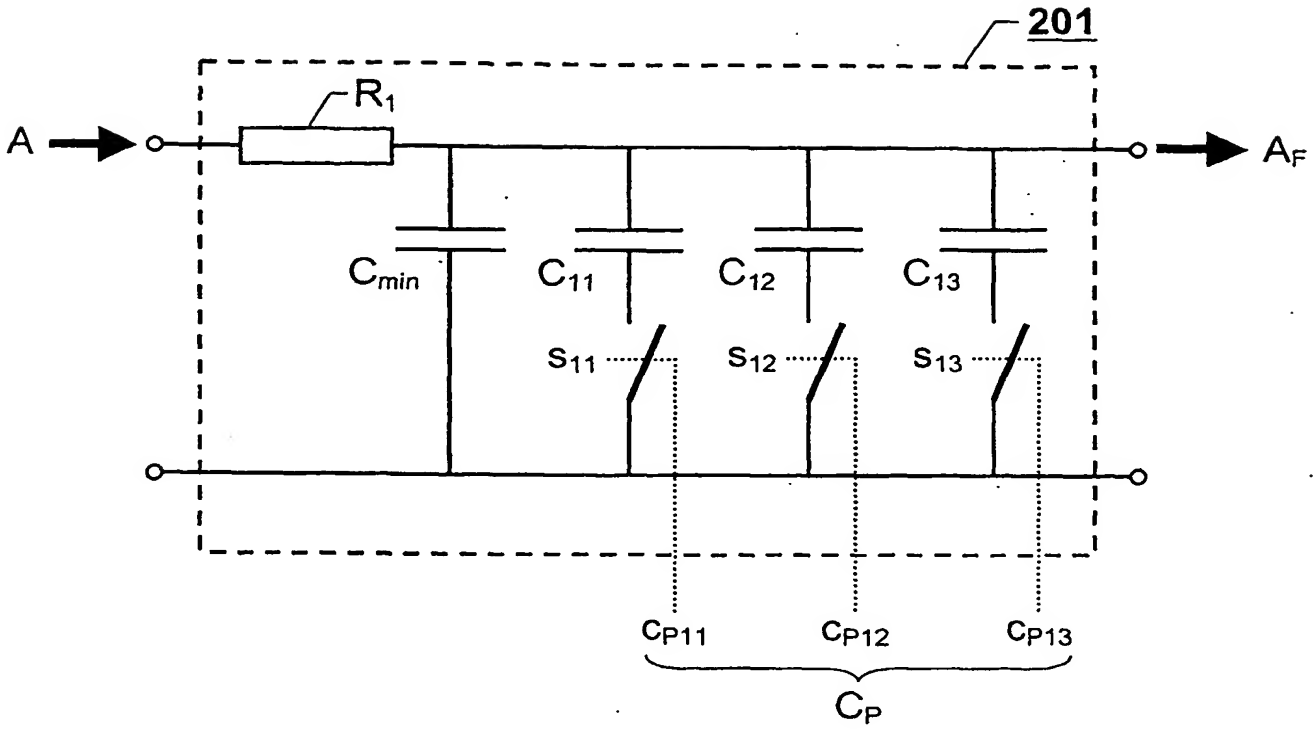
201
R1
A
AF
Cmin
C11
C12
C13
S11
S12
S13
CP11
CP12
CP13
CP

Fig. 1

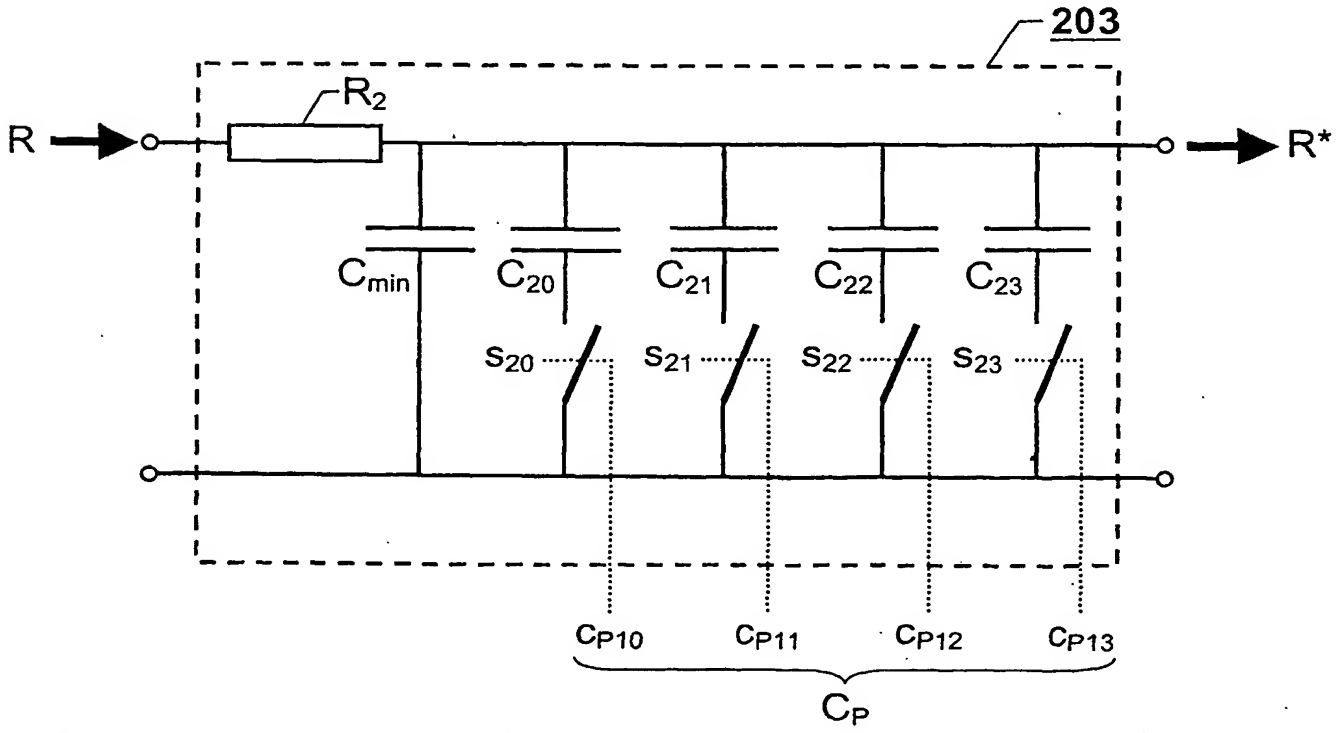
203
R2
R
R*
Cmin
C20
C21
C22
C23
S20
S21
S22
S23
CP10
CP11
CP12
CP13
CP

Fig. 3

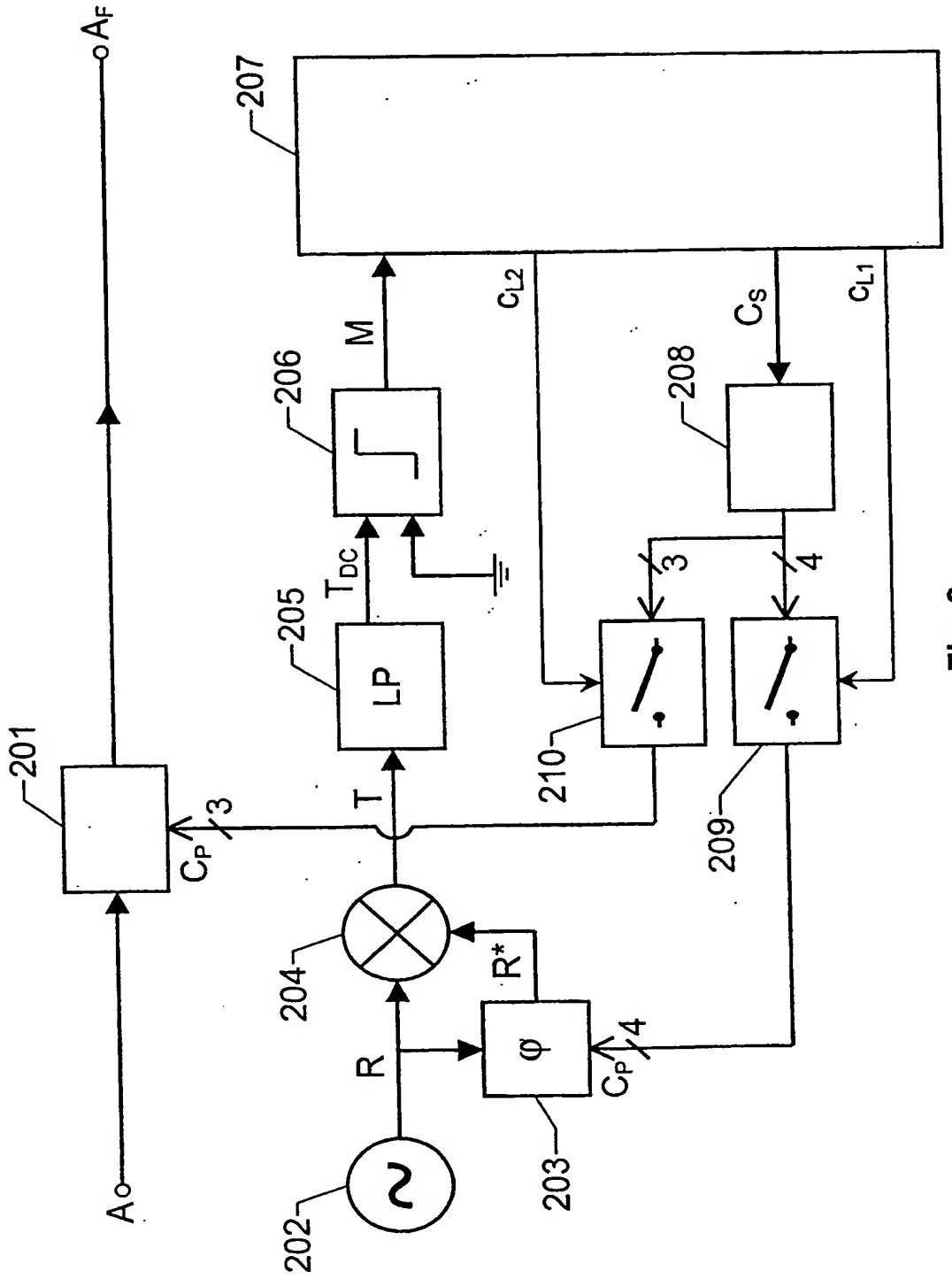
A_F
207
c_{L2}
C_S
c_{L1}
206
M
208
T_{DC}
205
LP
3
4
201
T
210
209
C_P 3
204
R*
R
φ
C_P 4
203
202
A

Fig. 2

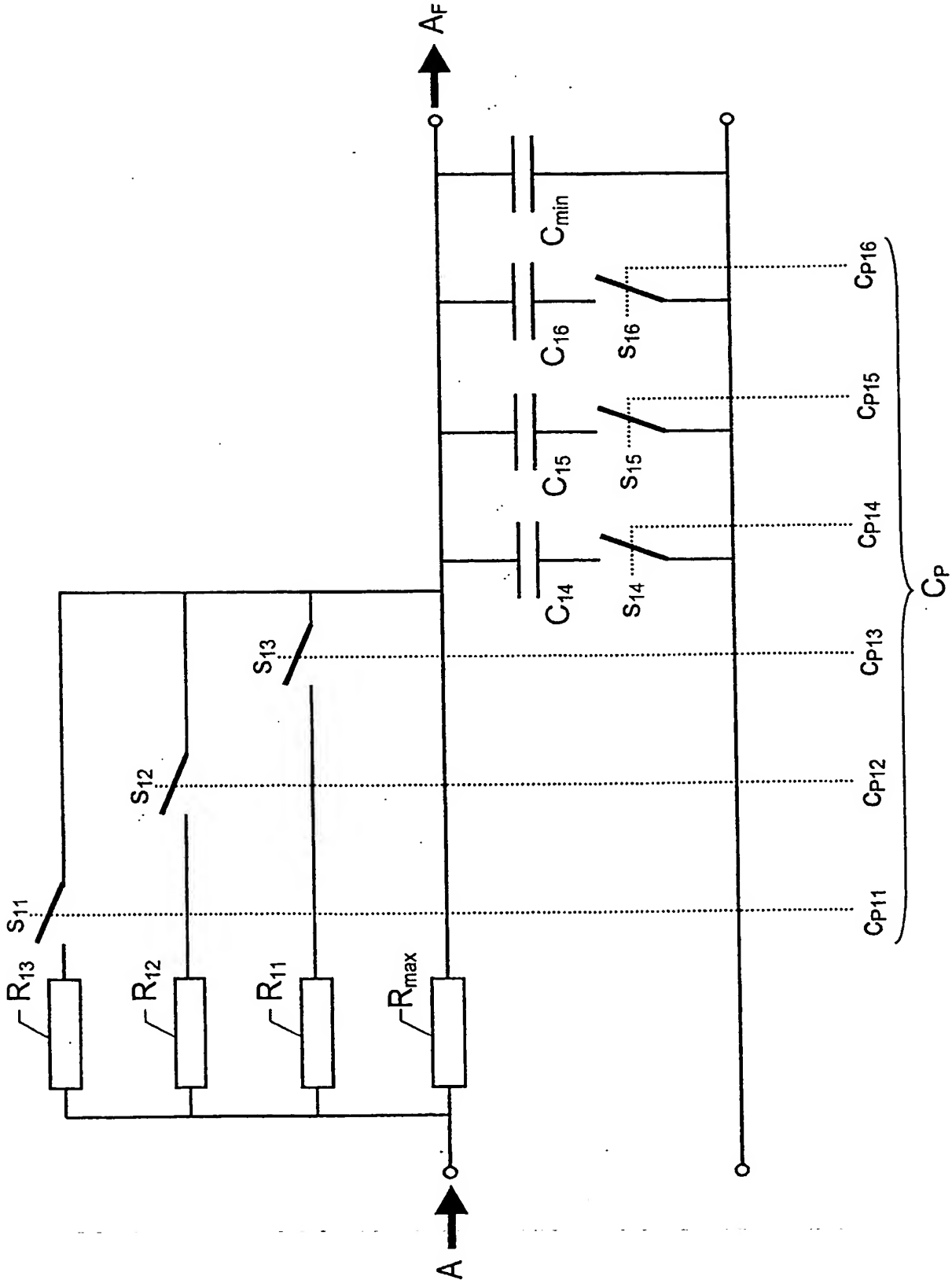
A
A_F
R13
R12
R11
Rmax
S11
S12
S13
S14
S15
S16
C14
C15
C16
Cmin
CP11
CP12
CP13
CP14
CP15
CP16
CP

Fig. 4

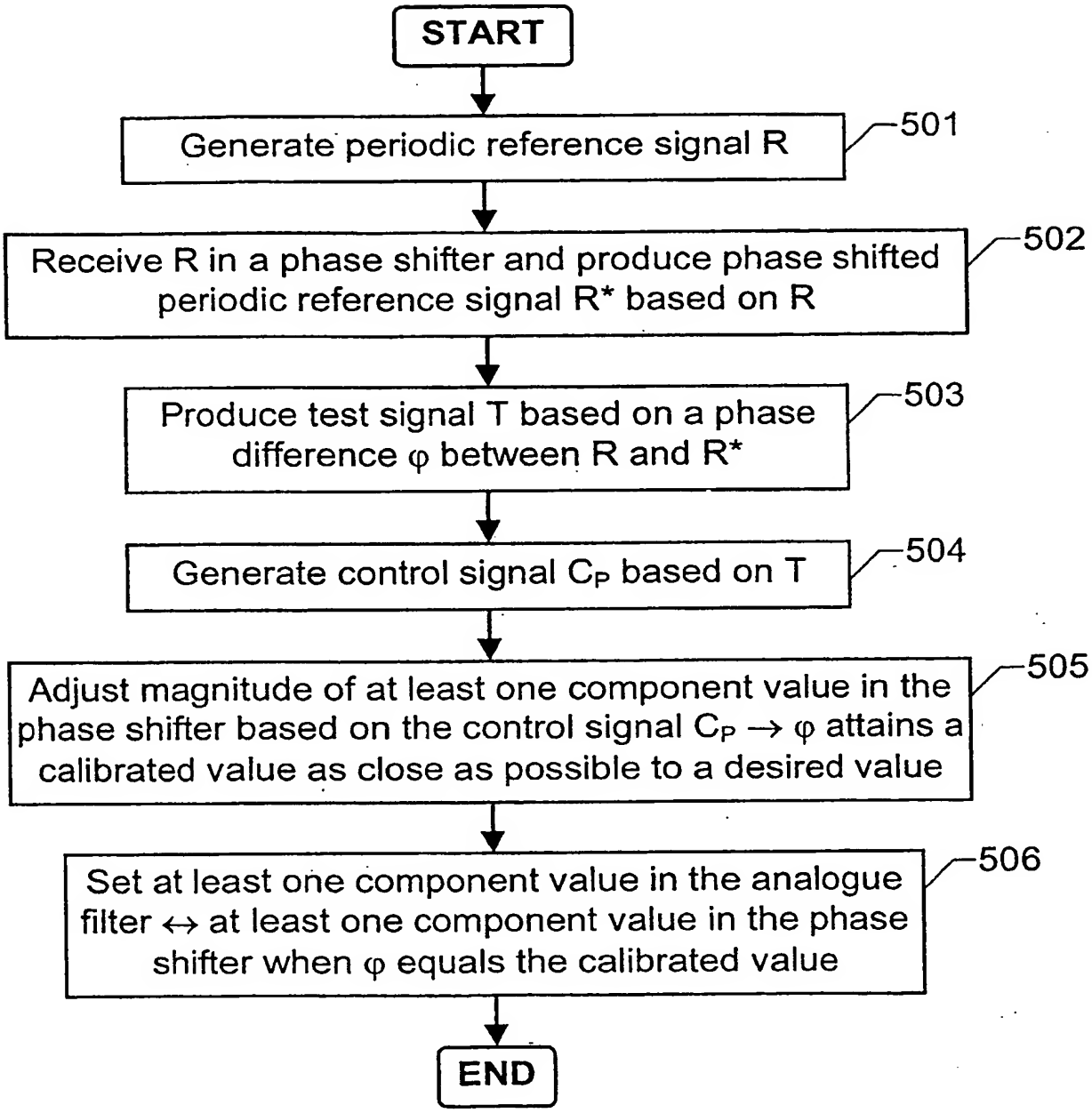
START
Generate periodic reference signal R
501
Receive R in a phase shifter and produce phase shifted periodic reference signal R* based on R
502
Produce test signal T based on a phase difference φ between R and R*
503
Generate control signal C_P based on T
504
Adjust magnitude of at least one component value in the phase shifter based on the control signal $C_P \rightarrow \varphi$ attains a calibrated value as close as possible to a desired value
505
Set at least one component value in the analogue filter ↔ at least one component value in the phase shifter when φ equals the calibrated value
506
END

Fig. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 02/00338

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: H03H 21/00
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: H03H, H03B, H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5245646 A (H. SPENCE JACKSON ET AL), 14 Sept 1993 (14.09.93) --	1-23
A	EP 0455156 A2 (SIEMENS AKTIENGESELLSCHAFT), 6 November 1991 (06.11.91) --	1-23
A	US 6169446 A (SERGE RAMET ET AL), 2 January 2001 (02.01.01) -- --------	1-23

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 May 2002	24 -06- 2002
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Stefan Hultquist/MN Telephone No. +46 8 782 25 00

Form PCT/ISA/210 (second sheet) (July 1998)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 02/00338

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5245646 A	14/09/93	NONE	
EP 0455156 A2	06/11/91	AT 101090 A	15/06/93
		AT 397166 B	25/02/94
US 6169446 A	02/01/01	EP 1027239 A	16/08/00
		FR 2775141 A	20/08/99